

Wafer Bump 3D AOI
Wire Bonding 3D AOI

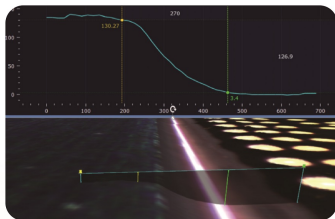
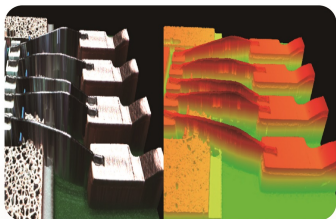
ZEUS *The Best 3D Technology*



ZEUS

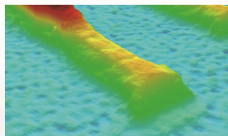
Wafer Bump & Wire Bonding 3D AOI

Technology and Features

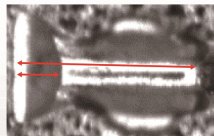
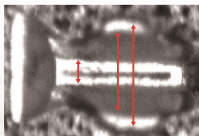


ZEUS was created on the basis of innovative 3D vision technology from PEMTRON as well as 15 years of experience that has enabled us to lead the semiconductor industry.

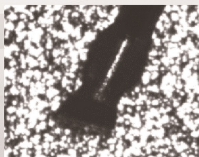
The experience and knowledge we have and our understanding of these kinds of technologies have resulted in a focus on the semiconductor industry in which we show the highest quality, performance and technology.



Precise 3D Image



Wire Lead Inspection

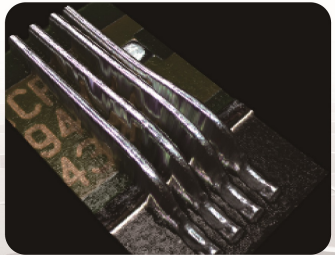
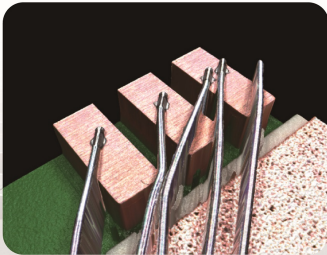
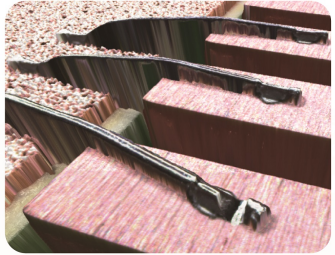
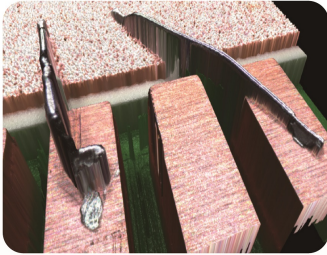


2D Image

The Best 3D WIRE Bonding AOI Inspection System

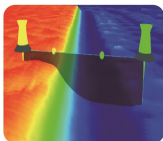
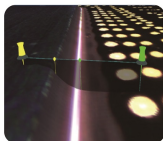
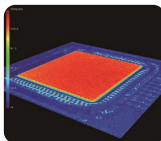
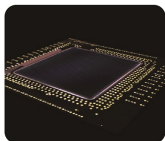
Inspection Capability

- ◉ Wire Missing
- ◉ Wire Broken
- ◉ Wire Down
- ◉ Wire Lift
- ◉ Damage
- ◉ Wire Bridge
- ◉ No Bond
- ◉ Loop Height
- ◉ Cut Wire
- ◉ Offset Wire Bond



The Best 3D Inspection System for Advanced Packaging

ZEUS is an inspection-optimized system which uses Moire' technology paired along with PEMTRON's own advanced optical technology



High accuracy die inspection without problems due to reflection

Main Features

Die inspection

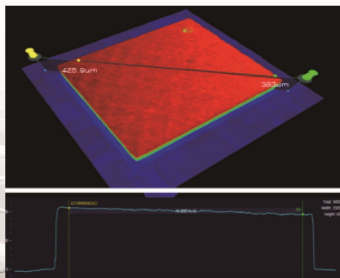
- reflective die surface inspection
- Integrated inspection review and analysis

3D inspection capability

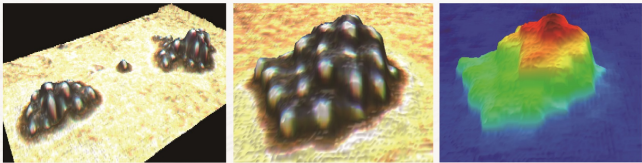
- Clear resolution
- Optimized image processing & algorithms

Applicable Packaging

SIP / FCBGA / FOWLP/ FOPLP/ WLCSIP



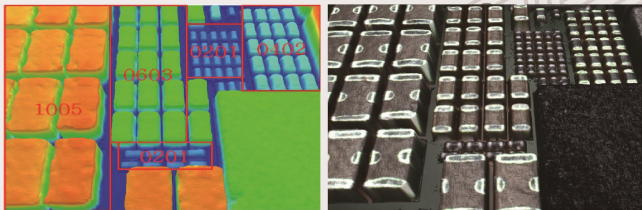
AOI + SPI Multi-Hybrid System



- ⬠ *Small component (Smaller than 008004) inspection*
- ⬠ *Integrated inspection review and analysis*
- ⬠ *True 3D inspection capability*
- ⬠ *Optimized image processing & algorithms*
- ⬠ *High Speed GPU and Image Processing*

Small Component Inspection Capability

- ⬠ *Solving your inspection challenges with superior innovations*



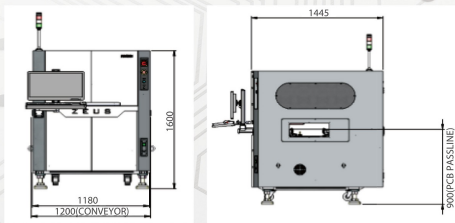
ZEUS (Wafer Bump & Wire Bonding 3D AOI)

SPECIFICATIONS

ZEUS	
Handling Media	Metal Carrier, JEDEC Tray, Wafer Ring Frame, Bare Wafer, Strip on Boat, Laminate
Package Types	SIP, FCBGA, FOWLP / FORPLP, WLCSFP
Inspection Types	Bump- Print Bump, Coined Bump, Solder ball Components: Capacitor & Resistor(Body, Solder Fillet, Joint, Body) Silicon Die Wire

Dimensions

1200 × 1445 × 1600 (WxDxH)
200~240AC, 50/60Hz single Phase, 5kgf/cm²



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